REMARKS

Claims 1-13 remain pending in this response.

Rejection of Claims 1-3 and 8-10 under 35 U.S.C. 102(e)

Claims 1-3 and 8 - 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Sartain et al. (US 6,169,747).

The present claimed invention recites a method and apparatus for controlling the bit rate of an output packet stream in a remodulator system. The apparatus includes a source of an input transport packet stream. An input packet buffer is coupled to the input transport packet stream source for generating a status signal indicating whether the input packet buffer is full, empty, or neither empty nor full. An output packet stream generator is coupled to the input packet stream buffer and responsive to an output clock signal, for generating the output packet stream in synchronism with the output clock signal. A variable output clock signal generator is responsive to a control signal and a control signal generator, responsive to the status signal, generates the control signal.

Sartain et al. dynamically compensates for differences in data rates for multistreamed systems wherein any or all of the streams in a multidimensional system may be individually compensated at one time. The status of an input buffer is monitored and used to change the number of oversamples within a frame of one of the number of streams. Alternatively, a high frequency clock in the system is used to stall one of the streams for one or more clock cycles. In both of the above described methods for compensating, the distortion due to differences in data rates is reduced.

Sartain et al. neither disclose nor suggest a variable output clock signal generator or a control signal generator for controlling the variable output clock signal generator in response to the status of the input packet buffer, as is recited in claims 1 and 8 of the present invention. Additionally, Sartain et al. neither disclose nor suggest generating the control signal so that the variable output clock signal generator increases its frequency if a status signal from an input packet buffer indicates that the input packet buffer is full or nearly full and decreases its frequency if the status signal indicates that the input packet buffer is empty or nearly empty, as is recited in claims 2, 3, 9 and 10 of the present invention.

Instead, Sartain et al. disclose an oversampled DAC system. An input buffer 111 holds input digital samples and generates a status signal indicating underflow, overflow, near underflow and near overflow conditions. Because a DAC system generates an analog signal having a level corresponding to the values of successive input samples, there cannot be a source of an input packet stream, nor an input packet buffer. Also because a DAC system generates an analog output signal, there cannot be an output packet stream generator generating the output packet stream in synchronism with an output clock signal, nor a variable output clock signal generator, nor a control signal generator controlling the output clock signal generator, as is recited in claims 1 and 8 of the present invention.

More specifically, Sartain et al. disclose a sample input buffer 111 which generates a status signal indicating whether it is full (overflow) or empty (underflow) or nearly full (near overflow) or nearly empty (near underflow). An interpolation filter interpolates a number (e.g. 128 in Sartain) of oversamples in a frame between each input sample received from the input buffer 111. In order to minimize overflow and/or underflow of downstream circuitry, the interpolation filter is controlled in response to the status of the input buffer 111 to vary the number of interpolated oversamples in a frame. In one embodiment (Fig. 6), the coefficients of a variable interpolation filter 145 are varied to change the number of oversamples in a frame (col. 4, lines 28-35). That is, depending on the state of the input buffer 111, either more (e.g. 129) or fewer (e.g. 127) oversamples are produced in a frame (col. 4. lines 60-66). In another

embodiment (Fig. 7) of Sartain et al., a fixed number (e.g. 128) of oversamples are produced by the interpolation filter 143 but some oversamples are either repeated or dropped (col. 5, lines 12-19). In yet another embodiment (Fig. 8) of Sartain et al., a fixed number of oversamples (e.g. 128) are produced by the interpolation filter 149, but a master clock 151 is stalled for one or more clock cycles depending on the status of the input buffer 111 (col. 5, lines 62-67). There is no disclosure or suggestion of an output packet stream generator responsive to a variable output clock signal generator as is recited in the present claimed invention.

Additionally, the Examiner states that the master clock 151 disclosed by Sartain et al. is analogous to the output clock signal generator as recited in claims 1 and 8 of the present claimed invention. However, as discussed above, the master clock 151 of Sartain et al. stalls when an overflow condition occurs and allows the system to remove the overflow condition (see col. 5, lines 62- 67). Sartain et al. neither disclose nor suggest "a variable output clock signal generator" as in the present claimed invention. Sartain et al. also neither disclose nor suggest "an output packet stream generator... responsive to an output clock signal" as in the present claimed invention. Furthermore, Sartain et al. neither disclose nor suggest "generating the output packet stream in synchronism with the output clock signal" as in the present claimed invention. Rather, Sartain et al., as stated above, stall the master clock signal to correct the overflow oversamples and remove the overflow condition (col. 5, lines 64-67).

In view of the above remarks regarding claims 1-3 and 8-10, it is respectfully submitted that the present claimed invention is not anticipated by Sartain et al. As claims 2 and 3 are dependent on claim 1 and claims 9 and 10 are dependent on claim 8, it is respectfully submitted that claims 2, 3, 9 and 10 are allowable for the same reasons discussed above with respect to claims 1 and 8. Thus, it is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

Rejection of Claims 4-7 under 35 U.S.C. 103(a)

Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sartain et al. (US 6,169,747) in view of Sato et al. (US 5,566,174).

As discussed above in detail, Sartain et al. neither disclose nor suggest "a variable output clock signal generator" as in the present claimed invention. Sartain et al. also neither disclose nor suggest "an output packet stream generator...responsive to an output clock signal" as in the present claimed invention. Furthermore, Sartain et al. neither disclose nor suggest "generating the output packet stream in synchronism with the output clock signal" as in the present claimed invention.

Sato et al. disclose a method of transmitting timing critical data, such as MPEG transport stream of packets, via an asynchronous channel. The packets are processed serially through a remuxer to obtain a constant rate and delivered to and consumed by one or more target decoders. To prevent overflow of the transport buffers inside these decoders, a single monitor-scheduler is provided for monitoring the transport buffers and delivering to each the packets wanted scheduled so as to avoid buffer overflow and loss of information. The method also includes restamping the transport packets with new PCRs.

Similarly to Sartain et al., Sato et al. neither disclose nor suggest a variable output clock signal generator, which varies the output clock signal in response to a control signal, which is generated in response to the status signal from the input packet buffer as in the present claimed invention. In addition, Sato et al. neither disclose nor suggest an input packet buffer which generates a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full, as is recited in Independent Claims 1 and 8. Instead, Sato et al. disclose a local clock 39 (Figs. 6 and 7) which produces a fixed output clock signal. There is no illustration of the local clock 39 being variable or receiving a control signal in Figs. 6 or 7, nor any such disclosure in the corresponding portion of the written description.

Claim 4 recites in pertinent part, "... if the status signal indicates that the input packet buffer is full, null packets are deleted from the input transport packet buffer." As discussed in detail above, Sato et al. neither disclose or suggest a variable output clock signal generator nor a control signal generator for controlling the variable output clock signal generator in response to the status of the input packet buffer, nor an input packet buffer generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 1. Also Sato et al. neither disclose nor suggest deleting null packets from the input transport packet buffer if the status signal indicates that the input packet buffer is full, as is recited in claim 4 of the present invention.

Instead, referring to Fig. 3, Sato et al. disclose circuitry 82 for unconditionally removing any null packet from the input packet stream (col. 5, lines 30-31). Furthermore, the buffer 42 of Sato et al. does not provide a status signal indicating that it is full. Instead, the status signal from buffer 42 indicates only that there is at least one packet in the buffer 42, i.e. whether the buffer is empty or not (col. 9, lines 45-46). Because Sato et al. already disclose circuitry for handling null packets in the input packet stream, there is no motivation to modify Sato et al. to handle null packets in a the manner recited in claim 4.

In view of the above remarks, it is respectfully submitted that Sato et al. when taken alone or in combination with Sartain et al. does not make the present invention as claimed in claim 1 unpatentable. As claims 4-7 are dependent on claim 1, it is respectfully submitted that claims 4-7 are allowable for the same reasons discussed above regarding claim 1. Thus, it is respectfully submitted that this rejection has been satisfied and should be withdrawn.

Claims 11 and 13 are rejected under 35 U.S.C. 103(a)

Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sartain et al. (US 6,169,747) in view of Kostreski et al. (US 5,734,589).

As discussed above in detail, Sartain et al. neither disclose nor suggest "a variable output clock signal generator" as in the present claimed invention. Sartain et al. neither disclose nor suggest "an output packet stream generator...responsive to an output clock signal" as in the present claimed invention. Furthermore, Sartain et al. neither disclose nor suggest "generating the output packet stream in synchronism with the output clock signal" as in the present claimed invention.

Kostreski et al. also neither disclose nor suggest generating a status signal indicating whether an input packet buffer is full, empty or neither empty nor full, nor generating a variable output clock signal in response to a control signal, nor generating the control signal in response to the status signal, as is recited in claim 8 of the present invention.

Instead, Kostreski et al. discloses a television and digital signal (audio, video, data) distribution system. The essence of Kostreski et al. is that set top boxes at consumer locations include a processor which can receive programs and data dynamically via one or more channels transmitted through the distribution system. Referring to Fig. 3 therein, analog television signals are received in analog AM-VSB form (316), digital television signals are received in MPEG format (318), and other digital signals are received in ATM packets (401), possibly modulated in any one of several disclosed formats: QPSK, QAM, VSB, etc. The television and digital signals are converted to RF channels and combined (315), and then supplied (303) to a distribution network (309, 311) in any one of several disclosed formats, which may be different from the format in which the data was received. While the presence of input packet buffers in the system of Kostreski et al. may be implied by the illustrated packet processing, there is no disclosure of any method for controlling the timing of the processing of those packets, and in particular no disclosure or suggestion of generating a variable output clock signal as in the present claimed invention. More specifically, there is no disclosure or suggestion of generating a variable output clock signal responsive to a control signal, nor generating a control signal in response to the status signal from an input packet buffer, nor generating an input packet buffer status signal

indicating whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8 of the present invention.

In view of the above remarks, it is respectfully submitted that Kostreski et al. when taken alone or in combination with Sartain et al. does not make the present invention as claimed in claim 8 unpatentable. As claims 11 and 13 are dependent on claim 8, it is respectfully submitted that claims 11 and 13 are allowable for the same reasons as discussed above regarding claim 8. Thus, it is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

Rejection of Claim 12 under 35 U.S.C. 103(a)

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sartain et al. (US 6,169,747) in view of Horton (US 5,969,770).

As discussed above in detail, Sartain et al. neither disclose nor suggest "a variable output clock signal generator" as in the present claimed invention. Sartain et al. also neither disclose nor suggest "an output packet stream generator...responsive to an output clock signal" as in the present claimed invention. Furthermore, Sartain et al. neither disclose nor suggest "generating the output packet stream in synchronism with the output clock signal" as in the present claimed invention.

Horton neither discloses nor suggests generating an output packet stream in synchronism with the output clock signal, as is recited in claim 8 of the present invention. Because Horton does not disclose or suggest generating an output packet stream, it cannot disclose or suggest generating a variable output clock signal in response to a control signal, nor generating a control signal in response to the status of the input packet buffer, nor generating a status signal to indicate whether the input packet buffer is full, empty, or neither empty nor full, as is recited in claim 8 of the present invention.

Instead, Horton discloses a receiver for receiving a transport packet stream (1507) and processing the packet stream to produce the sound (2la, 21b) and image (19) of the selected television program, including selected on-screen display images produced from MPEG graphics information (1525-5) previously stored in the ROM 1525. Input packets are received and stored in an input packet buffer 1513, the data in the packets is then extracted and used to produce the sound and image of the television program. MPEG packets representing an on-screen display are stored in ROM 1525 and are processed in the transport processor 1507, as appropriate, to generate the on-screen display. There is no output packet stream as in the present claimed invention.

In view of the above remarks, it is respectfully submitted that Horton when taken alone or in combination with Sartain et al. does not make the present invention as claimed in claim 8 unpatentable. As claim 12 is dependent on claim 8, it is respectfully submitted that claim 12 is allowable for the same reasons as discussed above regarding claim 8. Thus, it is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the fee to Deposit Account 07-0832.

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